

Patent Claims:

1. Method of storing data words in a RAM module,
c h a r a c t e r i z e d by the following method steps:
producing a check bit word from at least one data word
when writing the at least one data word into the RAM
module,
storing the check bit word,
reading out the check bit word when reading out the at
least one data word from the RAM module,
regenerating the check bit word from the at least one
read-out data word,
comparing the read-out check bit word with the regenerated
check bit word and generating an error message if they do
not correspond.
2. Method as claimed in claim 1,
c h a r a c t e r i z e d in that the check bit word is
generated by determining parity bits.
3. Method as claimed in claim 2,
c h a r a c t e r i z e d in that a 2 bit parity word is
generated from each data word, and one parity bit is
respectively determined from each data halfword.
4. Method as claimed in claim 1 or 2,
c h a r a c t e r i z e d in that a parity word is
generated from a number of data words, and its parity bits
are respectively determined from equal digits of all data
words.
5. Method as claimed in claim 1,
c h a r a c t e r i z e d in that the check bit words
are generated by calculating CRC words.

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6. Method as claimed in claim 5,
c h a r a c t e r i z e d in that in each case a number
of data words are summed up to form a memory word, and an
associated CRC word is calculated therefrom.
7. Circuit configuration for storing data words in a RAM
module, c h a r a c t e r i z e d by:
a first circuit unit (21) for generating a check bit word
from at least one data word when writing and reading the
at least one data word, a number of registers (11i, 61i)
for the allocated storage of check bit words for the data
words, and a second circuit unit (22) by means of which,
when reading data words, the associated check bit word is
compared to the check bit word regenerated by the first
circuit unit (21), and for generating an error message (F)
if the check bit words do not correspond.
8. Circuit configuration as claimed in claim 7,
c h a r a c t e r i z e d in that the number of
registers is produced by first 2 bit parity registers
(11i), and one 2 bit parity register is associated with
each data word.
9. Circuit configuration as claimed in claim 7,
c h a r a c t e r i z e d in that the number of
registers is produced by CRC registers (61i), one CRC
register being associated in each case with four data
words.
10. Circuit configuration as claimed in claim 9,
c h a r a c t e r i z e d by a multiplexer (71) for
storing four data words as one memory word, and a CRC
arithmetic unit (73) for calculating the CRC word from a
memory word and for storing the CRC word in an associated
CRC register (61i, 74).

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11. Circuit configuration as claimed in claim 10,
c h a r a c t e r i z e d in ~~that~~ the data words are 32
bit words and the CRC words are 9 bit words.
12. Circuit configuration as claimed in any one of claims 7 to
11,
c h a r a c t e r i z e d by a second register (12) for
storing a check bit word, the bits of which are
respectively determined from equal digits of all data
words, and a third register (13) for storing a check bit
word which is determined from the contents of the second
register (12).

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